PVMaT Cost Reductions in the EFG High Volume PV Manufacturing Line

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ABSTRACT

Over its 3-year PVMaT 5A2 program, ASE Americas achieved significant advances in its EFG technology. We implemented the use of SPC and DoE to help raise cell efficiencies by 0.5% absolute. Plasma etching of as-cut wafer edges was introduced to reduce acid use and strengthen the wafer. Novel cell processing methods using rapid thermal processing were investigated. We demonstrated the growth of large diameter (50 cm) EFG cylinders 75-100 microns in wall thickness, and made solar cells of 13+% efficiency on curved wafers as thin as 150 microns. Development of a larger diameter octagon with 12.5 cm faces is in progress. Flexible manufacturing methods involving computer aided manufacturing were developed for our expanded factory format and larger size (10cm x15cm) EFG wafers introduced into our factory during wafer expansions from 4 to 20 MW. Diagnostic techniques for on-line process monitoring were developed in the areas of stress measurement, microcrack detection and octagon flatness measurement. High speed and low damage lasers for cutting of EFG tubes were evaluated, and a new laser system capable of 2x current cutting speeds tested in production. Encapsulant and backskin material improvements and lower cost module designs were introduced in manufacturing. Overall, we will exceed the 25% module variable cost reduction goals for our program when all technology improvements are implemented.

1. Introduction

ASE Americas is completing the last year of its 3-year PVMaT 5A2 program. The overall focus of the work was to develop manufacturing technology for EFG wafers which will achieve cost reductions in high volume manufacturing. During this time span, the EFG wafer manufacturing capacity in Billerica, MA has increased from 4 to 20 MW. Many of the new technology developments achieved in this subcontract have contributed toward improved manufacturing and lower costs in the EFG manufacturing line.

The work in the program is structured along three main tasks areas: Manufacturing Systems, Low Cost Manufacturing, and Flexible Manufacturing. A description of the objectives and accomplishments for each task follows in the following sections.

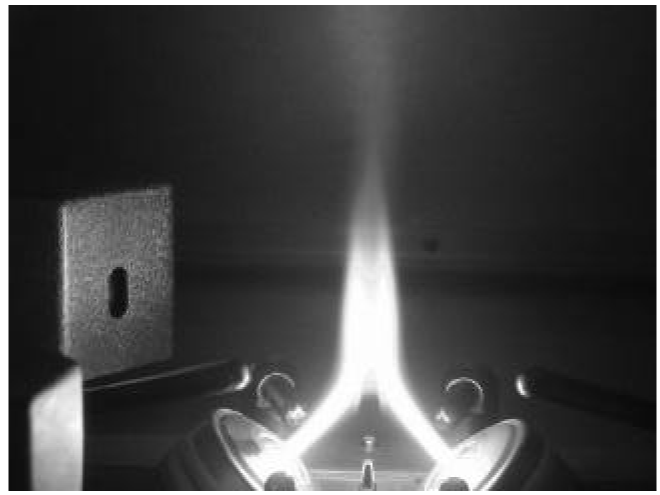

Figure 1. *Atmospheric Downstream Plasma™ [3] process for edge etching of laser-cut edges of EFG wafer stacks. Figure shows plasma flame which impinges on wafers held in carriers (not shown) rotated through the upper region of the flame. Reactant gas is introduced from below an argon flame, where it then dissociates into highly reactive ion species.*

2. Manufacturing Systems

This task has achieved its goal of reducing module variable production costs by 9%. Specific program objectives were: the implementation of computer aided manufacturing systems to aid in electrical and mechanical yield improvements (10% increase demonstrated in each area); development and implementation of ISO 9001 and ISO 14001 procedures leading to certification; and the reduction of chemical waste by 10%.

To improve electrical and mechanical yield, we have introduced customized SPC charts into the manufacturing line, including laser power for wafer cutting, sheet resistivity resistance for junction characterization, front metalization grid element widths, and interconnect bond strength. Design of Experiment matrices have continued on various process steps in the cell line to optimize AR coating and metal firing conditions.[1] Manufacturing line optimization has resulted in average line efficiencies of 14% and individual lots of 250+ cells exceeding 14.7%, with over 30% of the cells in these batches exceeding 15%. Documentation and Statistical sections of ISO 9001 procedures have been more than 80% completed. A Gap

Audit was carried out for ISO 14001 [2]; more recent efforts toward certification have focused on development of an environmental policy statement and work instructions for handling hazardous wastes.

We have introduced plasma etching of Si into our manufacturing line to reduce acid consumption (see Fig. 1). In this technology, coin-stacked wafers are placed in specially designed carriers and rotated through a plasma flame into which CF_4 is injected. Wafer carriers are rotated about their long axis for multiple runs, in order to expose all edges to the plasma. Etching rates of the wafer edges are significantly enhanced over conventional plasma processing. This process strengthens the wafer and reduces acid etch volume and resultant waste products by >50%.

3. Low Cost Manufacturing

This task had the objective of reducing costs through demonstration of: large diameter EFG tube growth, including thin wafer production (down to 100 microns) from EFG cylinders; development of advanced laser cutting systems for larger diameter EFG tubes–12.5 cm face octagons and thin cylinders; and demonstration of cell designs and processing technology capable of >15% efficiencies from thin wafers.

An EFG growth system was developed for production of 50 cm diameter cylinders. Solar cells of 13% efficiency and with thicknesses down to 150 microns were made on 6 cm x 6 cm area wafers cut from cylinders. [4] Continued development of this process was halted because of a lack of suitable large graphite die material and thermal stresses which prevented high yield cylinder cutting. We are using a heat transfer model to help in design of new hot zones for reducing stress in thin EFG tubes, and are implementing new diagnostic techniques developed for monitoring wafer properties to assist in this task. The large diameter EFG technology was redirected to development of a growth system for larger circumference (+25%) octagons and laser cutting station that will produce 12.5 cm x 12.5 cm wafers.

Manufacturing trials of several very high speed (>4x the standard speed of 25 mm/s) lasers were not successful. We have developed a 2x cutting speed laser, which has been tested on the production line. Evaluation of a low damage laser was completed for cutting of thin cylinder wafers with reduced levels of damage. Rapid Thermal Processing (RTP) methods have been studied to improve cell efficiencies and demonstrate increased throughput technology for thin EFG wafers. [5] EFG wafer bulk lifetime enhancement during RTP was studied in detail, which has guided cell process development in achievement of 15-16% cells made with RTP processing.

The new thin cylinder technology or new cell processing methods which could reduce EFG wafer costs by up to 50% could not be implemented because of unanticipated technical problems. Production of 12.5 cm square EFG wafers and laser cutting improvements are anticipated to result in module variable cost reductions of 5%. The shortfall in cost reductions targeted in this task is made up by the accomplishments in the following one.

4. Flexible Manufacturing

A module variable cost reduction of 5% was targeted for this task, but the development of new module materials and designs has increased this cost reduction to 16%.

The flexible manufacturing methods developed under this program helped to improve yields, throughput and automation levels in the 20 MW EFG factory format and allowed effective introduction of diversified product lines in wafers, cells and modules. These include new computer-aided data collection, integrated data bases, machine up time monitoring software, and SPC. They have permitted achievement of large capacity expansions in EFG wafers and diversification from 10 cm x 10 cm to 10 cm x 15 cm size wafers, and to manufacturing with new module designs without sacrificing quality, yield and throughput. These developments allowed us to achieve overhead cost reductions in manufacturing.

We further have worked on achieving continuous improvement of manufacturing processes through root mean cause failure analysis in wafer and module fracture, and module field performance. Module design improvements include a new encapsulant, new backskin to replace costly back glass, glass qualification, and reduction of lamination process times.

5. Conclusions

We have sustained manufacturing line efficiency levels of 14%, which were demonstrated during the first half of this program. A new plasma etching process for wafer edges has reduced the need for extensive acid etching and reduced waste generation. Laser development has resulted in new technology capable of a 2x speed enhancement. A larger diameter octagon and cutting station is being developed for production of 12.5 cm x 12.5 cm area EFG wafers. We have identified factors in EFG cell design which limit cell efficiency and have demonstrated 15+% cells using RTP.

Module variable cost reductions from the work carried out in this program will exceed 25%, and thus meet goals for this 3-year program at ASE Americas.

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